ABSTRACT

A processor integrated circuit capable of executing more than one instruction stream has two or more processors. Each processor accesses instructions and data through a cache controller. There are also multiple blocks of cache memory. Some blocks of cache memory may optionally be directly attached to particular cache controllers. The cache controllers access at least some of the multiple blocks of cache memory through a high speed interconnect, at least one of the these blocks being dynamically allocable to more than one cache controller. A resource allocation controller determines which cache memory controller has access to the at least one dynamically allocable cache memory block. In an embodiment the cache controllers and cache memory blocks heretofore described are associated with second level cache, each processor accesses the second level cache controllers upon missing in a first level cache of fixed size. The associated method provides for billing of processor time according to the amount of cache allocated to processors associated with a particular partition of a machine containing at least one processor integrated circuit having allocable cache.